1st Call for Paper

8th International Symposium on Control of Semiconductor Interfaces

November 27(wed)-30(Sat), 2019

Laboratory for Nanoelectronics and Spintronics,

Research Institute of Electrical Communication, Tohoku University, Sendai, Japan

Hosted by the 154 Committee on Semiconductor Interfaces and Their Application, The Japan Society for the Promotion of Science (JSPS) in cooperation with the 131 Committee on Thin Films, JSPS and supported by Research Institute of Electrical Communication, Tohoku University and The Japan Society of Applied Physics

http://iscsi8.org/

The Eighth International Symposium on Control of Semiconductor Interfaces (ISCSI-VIII) will be held in Sendai, Japan, on Nov. 27-30, 2019. ISCSI is a series of highly successful meetings starting at Karuizawa, Japan, in 1993. The aim of this symposium is primarily to bring together leading-edge researchers and other interested parties in the field of science and engineering of semiconductor interfaces and related matters. Joint sessions with the International Workshop on New Group IV Semiconductor Nanoelectronics will be arranged.

Topic Areas

Thin Film Growth and Characterization

Si, Strained Si, Ge, SiGe(C), SiC, Diamond, Silicide, Compound semiconductors
III-nitrides, Oxide semiconductors, High-k insulator, Low-k insulator
CVD, MBE, Selective epitaxy, Atomic layer control, Novel growth technique
Band engineering, Defect engineering, Simulation and modeling

Surface and Interface Control

Surface passivation and modification, Surface and interface chemistry, Schottky and ohmic contacts
Atomic scale characterization of surfaces and interfaces
Surface/interface issues in advanced devices

Formation and Characterization of Nanostructures

Nanodots, Nanowires, Superlattice, 2D materials, Self-assembling, Self-organization
Nanoscale characterization, In-situ characterization

Process and Device Technology

Impurity diffusion, Dry etching, Microfabrication, Isolation
SiGe gate, Source/drain and channel engineering, Base/emitter engineering
SOI, SGOI, III-V on Si, Wafer bonding, Virtual substrates and their Manufacturing
CMOS, HBT, BiCMOS, FeRAM, MODFET, SET, RTD, LED, LD, OEIC

Submission of Papers

Paper acceptance is based on the submitted abstract. The work must be original and unpublished. Prospective authors should submit abstract(s) (only in PDF file), two pages in length including all figures and tables, by **July 16 (Tue), 2019**, to a submission World Wide Web site (site information will be announced at http://iscsi8.org/). The two-page abstract must be written in English and typed in an area of 8.5 x 11 inches or A4 size. The first page must be headed by the title of the paper, author(s), affiliation(s), address, telephone number, e-mail address of the corresponding author. The text of the abstract must be written to clearly and concisely explain the specific results of the work and its originality. Please refer to the sample abstract (PDF file at http://iscsi8.org/) for detailed format information. An abstract template (Microsoft Word) is available at http://iscsi8.org/, and please follow the instructions for preparation of your abstract(s). Proceedings will be published in a special issue of Elsevier Journal, **Materials Science in Semiconductor Processing**.